

TST-03

User's Manual

Bear Technologies
www.beartech.com.tw

Product Feature :

- ISA Slot Test
- CMOS Data Setup

Product Content :

- TST-03 Test Card * 1



Common Program Syntax :

- Filename : MB2.EXE & CMOS.COM

MB2.EXE Syntax

```

MB2 [/????]

+Z: 0ws Test +N:IOCHCK# Test +10:IOCHRDY# Test
+F: REFRESH# Test +0: OSC Test +A: ATCLK Test +S: SA[15:0] Test
\IRQ:All IRQ?? Skip \DMA:All DRQ? Skip
/????: Lap Count /1: Lap Count = 1 ISA: Test ISA Slot Only (01> .. 39>)
P2: I/O[0320h:0337h]&[3338h:333Bh] Default:[0320h:0337h]&[0338h:033Bh]
Tnn: Timer test Tolerance T08: 8/1070 T05 ( Default)
\2: SMEM?#/MEM?# Skip \5: IOCS16# Skip \6: MEMCS16# Skip \7: -5V Skip
\8: -12V Skip \9: +12V Skip \13: BALE Skip \39: SA[19:0] CPU Skip
\M: MASTER# Skip \W: MASTER MEMW# Skip \L: LA[23:17],SA16 Skip
\I03: IRQ3 Skip \I04: IRQ4 Skip \I05: IRQ5 Skip \I07: IRQ7 Skip
\I10: IRQ10 Skip \I11: IRQ11 Skip I09: IRQ9 Test I12: IRQ12 Test
I14: IRQ14 Test I15: IRQ15 Test \D00 : DRQ00 Skip \D01: DRQ01 Skip
\D03: DRQ03 Skip \D05: DRQ05 Skip \D06: DRQ06 Skip \D07: DRQ07 Skip
\DR : DMA Memory Read -> I/O Write Skip \B: Speaker Test Skip
\R : CMOS RAM Skip \G: GateA20 Skip \D: 46> Skip D: 46> Tolerance++
F : Fast GateA20 K: 0042 GateA20 M: DRQ7 Generate Master# (Def: DRQ5)

MB2 /1 \I03 \M ISA ; 01> .. 39> Test (IRQ3 Skip , MASTER# Skip)

```

MB2.EXE

```

ISA SLOT TEST (TST-02) Ver 1.60 07/03/2000 Bear Technologies (? : Help)
Lap count : 0001 (I/O Port 0320h->0337h) S_time:01/01/1997 00:03:40
Loop count : 0001 (I/O Port 0338h->033Bh) C_time:01/01/1997 00:03:50

01> RESEYDRU : Pass 19> IRQ 10 : Pass 37> LA[23:16] MST: Pass
02> SMEMW#/R# : Pass 20> IRQ 11 : Skip 38> SA[15:0] MST: Skip
MEMW#/R# 21> IRQ 12 : Skip 39> SA[19:0] CPU: Pass
03> IOW#,IOR# : Pass 22> IRQ 14 : Skip 40> IRQ 08 : Pass
04> SD[15:0] : Pass 23> IRQ 15 : Skip 41> Timer(1070)05: 1069
05> IOCS16# : Pass 24> REFRESH# : Skip 42> Speaker : Test
06> MEMCS16# : Pass 25> OSC : Skip 43> Cmos Ram(128): Pass
07> -5V : Pass (14.318 +/- 5%) 44> A20 Gate : Pass
08> -12V : Pass 26> ATCLK(5-12M) : Skip 45> Cache Compare: Skip
09> +12V : Pass 27> DRQ0,DACK0# : Pass 46> Timer(5B/5CH): 05BH
10> IOCHRDY# : Skip 28> DRQ1,DACK1# : Pass
11> IOCHCK# : Skip 29> DRQ2,DACK2# : Skip
12> 0WS : Skip 30> DRQ3,DACK3# : Pass
13> BALE : Pass 31> DRQ5,DACK5# : Pass
14> IRQ 03 : Pass 32> DRQ6,DACK6# : Pass
15> IRQ 04 : Pass 33> DRQ7,DACK7# : Pass
16> IRQ 05 : Pass 34> AEM : Pass
17> IRQ 07 : Pass 35> TC : Pass
18> IRQ 09 : Skip 36> MASTER#,SBHE : Pass

Co_Processor: Present
Cache Size(20): 512 K 074
Base Memory : 640 K
Ext Memory : 261108 K

Results ("Q" : Quit)

Pass

```

CMOS.COM Syntax

```

CMOS SETUP (PCI??/USBT-02[W]/COMTST-01) Ver 2.5 01/11/2010 Bear Technologies

CMOS [R?][U??][C??][#Filename][T][D][A?][B?][?] [G]  ?:Help
R0 .. R3 (Read Mode)      0: M.B. 1: U49 2: U50 3: File
U01 .. U31 (Update Mode) C01 .. C32 (Compare Mode)
01: M.B.-> U49   02: M.B.-> U50   03: M.B.-> File  10: U49 -> M.B.
12: U49 -> U50  13: U49 -> File  30: File-> M.B.  31: File-> U49
A0 .. A5 (FDD A: Type)   0:None 1:360K 2:1.2M 3:720K 4:1.44M 5:2.88M
B0 .. B5 (FDD B: Type)   0:None 1:360K 2:1.2M 3:720K 4:1.44M 5:2.88M
T :Update TIME/DATE Only  D :Update CMOS DATA Only Index[0Eh ..7Fh]
CMOS                      ;Read M.B. CMOS DATA
CMOS R1                   ;Read U49 CMOS DATA
CMOS R3 #C:\TST-02\RTC.1 ;Read C:\TST-02\RTC.1
CMOS U01                  ;Copy M.B. CMOS DATA to U49
CMOS U03 #A:BX01.1       ;Copy M.B. CMOS DATA to A:BX01.1
CMOS U10                  ;Copy U49 CMOS DATA to M.B.
CMOS U13 #A:BX01.1       ;Copy M.B. CMOS DATA to A:BX01.1
CMOS U30 #A:BX01.1       ;Copy A:BX01.1 to M.B.
CMOS C30 #A:BX01.1       ;Compare A:BX01.1 with M.B.
CMOS A0                   ;SET M.B. FDD A: None & Read CMOS
  
```

CMOS.COM SETUP

```

CMOS SETUP (PCI??/USBT-02[W]/COMTST-01) Ver 2.5 01/11/2010 Bear Technologies
Date   : 01-01-2097      Paralle Port: 0378h      156> Compare   : Pass
Time   : 00:04:51      Operate Mode: Update    157> Check_Sum : Pass
FDD A  : 1.44 M         Source   : 70H/71H M.B.
FDD B  : None          Target   : U49          SET-PCI or TST-02 .....

CMOS [R?][U??][C??][#Filename][T][D][A?][B?][?]  C1/C2:COMTST-01
R0 .. R3 (Read Mode)  U01 .. U31 (Update)  C01 .. C31 (Compare)
0:M.B. 1:U49 3:File  T:Update Time only D:Update DATA only
CMOS    ;Read M.B.          CMOS U01 ;Update M.B. to U49
CMOS U03 #C:\bear\bx01.B1 ;Update M.B. to C:\bear\bx01.B1
  
```

	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00H	51	BF	04	F7	00	FF	00	01	01	97	26	02	50	80	00	00
10H	40	E1	F0	02	0F	80	02	C0	FF	2F	2F	30	FF	FF	00	00
20H	00	00	00	00	00	00	FF	3F	10	FF	FF	FE	3F	3F	0B	B7
30H	C0	FF	20	FF	FF	FF	FF	FF	FF	FF	FF	0B	F0	D1	F8	17
40H	80	FB	FD	FC	88	80	00	B8	FE	FF	BB	4D	28	FC	FC	FF
50H	80	FF	F0	F0	FF	17	FC	FF	00	00	20	00	C0	C0	BF	FF
60H	FF	FF	FE	34	FC	FF	FF	2F	00	00	00	00	00	00	00	00
70H	2F	00	00	00	00	00	00	00	00	FF	16	83	FF	FF	FF	FF

Test Principle :

A. Product Feature:

- ISA Slot Test
+5V , -12V , +12V , -5V , SD[15:0] , IOW# , IOR# , MEMR# , MEMW# ,
SMEMR# , SMEMW# , IOCS16# , MEMCS16 , BALE , IRQ3 , IRQ4 ,
IRQ5 , IRQ7 , IRQ10 , IRQ11 , DRQ0 , DRQ1 , DRQ3 , DRQ4 , DRQ5 ,
DRQ6 , DRQ7 , AEN , TC , MASTER# , SBHE , SA[19:0] , LA[23:16]

B. Compatibility:

- MB , IPC

D. Testing Procedure:

1. TST-03 Test Card Connect To ISA Slot
2. Boot the screen to DOS platform
3. Excute **MB2.EXE**

<http://www.beartech.com.tw>
Bear Technologies
TEL : (02)2649-9000