TRACE-PCI
STEP-LPC
TR-ISA

Operation Manual

Bear Technology Co., Ltd.

TRADEMARKS

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. IOR#, IOW#, MEMR# or MEMW# can be selected as single-step condition

. LA[23:20] ,SA[19:0] 7-segment display

SA[15:0] 7-segment display

. ERROR CODE 7-segment display

. 8 LEDs displays the status of following important singals of ISA

IOR#/IOW#/MEMR#/SMEMR#/MEMW#/SMEMW#/AEN/IOCHRDY

1-2> Description of Functions

A> ERROR CODE:

Displays the content of I/O PORT 80H

For example: MOV AL,5AH

OUT 80H,AL

Execute the above two commands and ERROR CODE will display SAH

B> Address Display

It contains 6 7-sgement displays

It displays ADDRESS BUS LA[23:20], SA[19:0], a total of 24 ADDRESS Lines

C> Data Line Display

It contains 4 7-sgement displays

It displays DATA BUS SD[15:0], a total of 16 DATA Lines

D> Control Signal LED Display

It displays the following 8 control signals of ISA:

IOR#,IOW#,MEMR#,SMEMR#,MEMW#,SMEMW#, AEN,IOCHROY#

E> When Single-Step Execution Function is enabled, the LED next to the switch will go on

F> R.C. (automatic) drive settings and LED:

When Single-Step Execution Function is Activated, the LED next to the switch will go on

Single-Step Execution Switch	R.C. (automatic) drive switch	description of function
switched up (DISABLE)	X	FREE RUN

At least one of the following sets is on(switched right): SW8 IOR#/IOW#/MEMR#/MEMW#

Single-Step Execution Switch	R.C. (automatic) drive switch	description of function
switched down (ENABLE)	switched up (DISABLE)	manual single-step execution
switched down (ENABLE)	switched down (ENABLE)	automatic single-step execution

F> Single-Step Execution Button

When single-step conditions are met, IOCHRDY# will become LOW and current ISA CYCLE will be in WAIT STATE until the button is pushed to complete the current ISA CYCLE

Single-Step drive button is functional on the condition that at least one of the following is ON (switched right):

SW8 IOR#/IOW#/MEMR#/MEMW#

Single-Step Execution Switch	R.C. (automatic) Drive Switch	Funciton Description
switched down (ENABLE)	switched up (DISABLE)	manual single-step execution

1-3> Switch Settings:

SW8: single-step condition setting

SW8-1 ON : MEMW# single step
SW8-2 ON : MEMR# single step
SW8-3 ON : IOW# single step
SW8-4 ON : IOR# single step

SP1: single step execution (SINGLE STEP) ENABLE/DISABLE

switched up: single step execution function disabled
switched down: single step execution function enabled

SP3: R.C. (automatic) drive setting: ENABLE or DISABLE

switched up: R.C. (automatic) drive disabled
switched down: R.C. (automatic) drive enabled

PU1: manual single-step drive button(STEP TRIGGER)

When to use?

When single-step conditions are met，and ISA CYCLE is in the WAIT STATE ，push the button will cleartheWAIT STATE

TR-ISA Professional

2-1> Introduction to its Functions

Single-Step Execution Function

Address interrupt point

Address interrupt point + Data interrupt point

Address interrupt point +SA[4:0] No-comparison function

Manual drive and RC drive function

. Force IOCHRDY# to LOW and intercept the first ISA cycle from the main board

. LA[23:20] ,SA[19:0] 7-segment dispaly

. SD[15:0] 7-segment display

. ERROR CODE 7-segment displa. ERROR PORT (SOH,190H,300H) can be set usgin switch

2-2> Description of Functions

A> ERROR CODE:

It shows the content in I/O PORT (80H, 190H or 300H)

For example: MOV AL,5AH

OUT 80H,AL

Execute the fore-mentioned two commands then ERROR CODE will display 5AH,

B> Address Display

It contains 6 7-segment displays for ADDRESS BUS LA[23:20], SA[19:0], a total of 24 ADDRESS Lines

C> Data Line Display

It contains 4 7-segment displays for DATA BUS SD[15:0], a total of 16 DATA Lines

D> Control Signal LED Display

It displays the following 14 control signals of ISA

IOR#,IOW#,MEMR#,SMEMR#,MEMW#,SMEMW#,SAO,SBHE,IOCS16#

MEMCS16#,REFRESH#,AEN,IOCHRDY#,MASTER#

E> Single-Step Execution Switch and LED

When Single-Step Execution Function is enabled, the LED next to the switch will go on

F> Address Interrupt Point Switch and LED

When Address Interrupt Point Function is enabled, the LED next to the switch will go on

G> DATA Interrupt Point Switch and LED

When DATA Interrupt Point Function is enabled, the LED next to the switch will go on

H> Interrupt Point Switch Address Switch

It can set Address Interrupt Point SA[19:0]

I> DATA interrupt point setting switch

It can set DATA interrupt point SD[15:0]

J> interrupt point SA[4:0] settings for comparison

SA4X:

ON: SA4 will not be compared

OFF: SA4 will be compared

SA3X:

ON: SA3 will not be compared

OFF: SA3 will be compared

SA2X:

ON: SA2 will not be compared

OFF: SA2 will be compared

SA1X:

ON: SA1 will not be compared

OFF: SA1 will be compared

SA0X:

ON: SA0 will not be compared

OFF: SA0 will be compared

K> Settings of Conditions for Interrupt Point and Single-Step Execution

It can set 1>IOR# 2>IOW# 3>MEMR# 4>MEMW#, repectively, as the control condition for interrupt and single-step

L> Single-Step and Interrupt Point and Single-Step Drive Button

When single-step or interrupt point conditions are met, IOCHRDY# will become LOW and current ISA CYCLE will be in WAIT STATE until the button is pushed to complete the current ISA CYCLE

M> Single-Step and Interrupt Point RC Drive Switch

When making RC Drive settings, the WAIT-STATE that generated by single-step or interrupt point will clear automatically after 1/4 Sec

N> FORCE# Switch

When FORCE# is ON, IOCHRDY# will forced to be LOW, making ISA cycle in WAIT STATE

O> ERROR PORT Setting Switch

It can set I/O PORT of ERROR CODE to 8OH, 19OH or 30OH

1-3> Switch Setting

SP1: Single-Step (ENABLE/DISABLE)

switched up：Single-Step disabled

switched down：Single-Step enabled

SP2: Address Break Function (ENABLE/DISABLE)

switched up：Address Break function disabled

switched down：Address Break function enabled

SP3: DATA BREAK Function (ENABLE/DISABLE)

switched up：Data Break function disabled

switched down：Data Break function enabled

SP4:RC TRIGGER(drive) ENABLE/DISABLE

switched up：RC TRIGGER ENABLE

switched down：RC TRIGGER DISABLE

PU1: Manual Single-Step Drive Button (STEP TRIGGER)

When to Use? When RC Trigger is set to diabled and when single-step or interrupt point conditions are met while ISA CYCLE is in WAIT STATE, push this button will clear current WAIT STATE

STEP COMMAND：Control Condition for Interrupt Pointand Single-Step

ON (switched right)：ENABLED

OFF(switched left)：DISABLED

SW8-4: IOR#

SW8-3: IOW#

SW8-2: MEMR#

SW8-1: MEMW#

SW2[5:1]： Address interrupt point +SA[4:0] No-comparison selection

SW2-5:

ON(switched down): SA4 will not be compared

ON(switched up): SA4 will be compared

SW2-4:

ON(switched down): SA3 will not be compared

ON(switched up): SA3 will be compared

SW2-3:

ON(switched down): SA2 will not be compared

ON(switched up): SA2 will be compared

SW2-2:

ON(switched down): SA1 will not be compared

ON(switched up): SA1 will be compared

SW2-1:

ON(switched down): SA0 will not be compared

ON(switched up): SA0 will be compared

SW2[7:6]:ERROR PORT Address Selection

PSEL2(SW2-7)	PSEL1(SW2-6)	ERROR PORT
OFF(switched up)	X	80H
ON (switched down)	OFF(switched up)	190H
OFF(switched up)	OFF(switched up)	300H

SW2-8: FORCE# setting

ON(switched down): force IOCHRDY# to be LOW

OFF(switched up): no function

SW1:DATA interrupt point SD[7:0]

OFF(switched up):1 ON(switched down):0

SW1-8	7	6	5	4	3	2	1	0	
	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	
	ON	OFF	ON	OFF	OFF	ON	OFF	ON	5AH

SW7,SW6,SW5,SW4,SW3,ADDR interrupt pointSA[19:0] setting

OFF(switched up):1 ON(switched down):0

SW7:SA[19:16]

SW6:SA[15:12]

SW5:SA[11:8]

SW4:SA[7:4]

SW3:SA[3:0]

	SW7	SW6	SW5	SW4	SW3
80H	0000	0000	0000	1000	0000
C0000H	1100	0000	0000	0000	0000
378H	0000	0000	0011	0111	1000

3> TRACE-PCI

3.1> Product Features

. 8 7-segment displays that show PCI ADDRESS BUS.

. 8 7-segment displays that show PCI DATA BUS.

. 2 7-segment displays that show ERROR CODE of the main board.

1 toggle switch that is used to select the display mode of PCI DATA BUS between TRANSPARENT LATCHED

2 LEDs used to select the display mode of PCI DATA BUS between TRANSPARENT LATCHED

1 toggle switch that is used to select single tracking function of PCI TRDY# Count

1 LED used to indicate PCI TRDY# Count single tracking function is enabled

2 PUSH Wheel Switches used to the select single tracking function of PCI TRDY#

TRDY# Counter (1 .. 255).

1 toggle switch that is used to select single tracking function of PCI IOW#

1 LED used to indicate single tracking function of PCI IOW# Count is enabled

1 toggle switch that is used to select single tracking function of PCI IOW# (manual or automatic)

1 LED used to indicate automatic (R.C. Delay) single tracking function of PCI IOW# Count is enabled

. 1 Push Button used to trace LOW#Cycle PCI.

1 Push Button is connected to the Hardware Reset Pins of the main board throught 之 Pin Header of TRACE-PCI to conduct a Hardware Reset on the main board.

. 3 LEDs display IOR, IOW and MEMR CYCLE of PCI

. 4 LEDs (BE3#,BE2#,BE1#,BE0#) shows which bytes of PCI DATA BUS are valid.

3.2-3> Switch Setting

JP1: used to adjust timing of PCI ADDRESS LATCH

1 4 2-3(lower) : PCI ALE DELAY

◎ ◎

◎ ◎

2 3

1 4 1-4(upper) : PCI ALE NORMAL(default setting)

◎ ◎

◎ ◎

2 3

JP2: used to adjust the timing of PCI DATA LATCH.

1 4 2-3(lower) :PCI DATA LATCH DELAY

◎ ◎

◎ ◎

2 3

1 4 1-4(upper) :PCI DATA LATCH NORMAL(default setting)

◎ ◎

◎ ◎

2 3

JP3: POST-PCI State Machine Clock Source

◎1 1-2 : PCI Clock(default setting)

◎2

◎3

◎1 2-3 : External Oscillator

◎2 If mother board stop PCI CLOCK.

◎3

. SP1: It is used to selected the display mode of PCI DATA BUS.

switched up: PCI DATA BUS display mode is TRANSPARENT (PASS).

switched down: PCI DATA BUS display mode is LATCHED (LATCH).

SP4: It is used to selected the single-tracing function of PCI TRDY# Count .

switched up: PCI TRDY# Count single-step tracing function disabled

switched down: PCI TRDY# Count single-step tracing function enabled

SW2: PUSH Wheel Switch

TRDY# COUNTER [7:4]

SW1: PUSH Wheel Switch

TRDY# COUNTER [3:0]

Example:

SW2=0 SW1=3 TRDY# COUNTER = 03 H (3)

SW2=5 SW1=4 TRDY# COUNTER = 54 H (84)

SW2=F SW1=F TRDY# COUNTER = FF H (255)

SP3: It is used to select single-tracing function of PCI IOW#

It should be used with Bear Technology Debug BIOS (TR-ISA1.1M OR TR-ISA1.2M)

switched up: PCI IOW# Single-Step Tracing function disabled

switched down:PCI IOW# Single-Step Tracing function enabled

SP2: It is used to select single-step tracing function(manual or automatic) of PCI IOW#

It should be used with Bear Technology Debug BIOS (TR-ISA1.1M OR TR-ISA1.2M)

switched up:PCI IOW# single-step tracing function is in manual mode

switched down:PCI IOW# single-step tracing function is in automaticl mode(R.C. DELAY)

PU1: Push Butto)

When selecting manual mode for PCI IOW# single-step tracing function, push PU1 to trace next IOW# Cycle of PCI

BUT1 & JP4: Push Button

1 It is connected to the Hardware Reset Pins of the main board through the Pin Header (JP4) of TRACE-PCI. It is used to to conduct a Hardware Reset on the main board.

. Notice: Why is TR-PCI provided with two display modes of PCI DATA BUS?

PCI BUS main boards usually conduct conversion between AD[31:0] (PCI SIGNAL) and LA[23:17], SA[19:0] and SD[15:0] (ISA SIGNAL) through PCI TO ISA BRIDGE

A1> ISA WRITE CYCLE:

ADDRESS : AD[31:0]→LA[23:17],SA[19:0]

DATA : AD[31:0]→SD[15:0]

A2> ISA READ CYCLE:

ADDRESS : AD[31:0]→LA[23:17],SA[19:0]

DATA : SD [15:0]→AD[31:0]

A3> During ISA READ CYCLE, SD[15:0] will be converted to AD [31:0]. When using ISA Debug Card to conduct single-step execution function of ISA READ, most AD[31:0] on most main boards will directly reflect SD[7:0]; in this case, select TRANSPARENT mode for PCI DATA BUS

ISA BUS		PCI BUS	
LA[23:20],SA[19:0]	SD[7:0]	PCI ADDRESS	PCI DATA
FFFFF0	EA	FFFFFFF0	??????EA
FFFFF1	5B	FFFFFFF0	????5BEA
FFFFF2	E0	FFFFFFF0	??E05BEA
FFFFF3	00	FFFFFFF0	00E05BEA

A4> On some main boards on the marke(for example, INTEL ?X), SD[7:0] will not be directly reflected to AD [31:0]. In these cases, select LACHTED mode for PCI DATA BUS.

…Notieces……

1> When the main board is executing 32-bit FETCH CODE CYCLE, HOSt will send 32-bit MEMR CYCLE to PCI BUS.

But snice the ADDRESS Decoding is ISA CYCLE, so 4 times of 8-bit (or 32-bit) ISA MEMR# CYCLE will be performed and then converted to D[31:0] of CPU through AD[31:0] of PCI.

So theoretically, as long as the 4th-time ISA MEMR# CYCLE and TRDY# & IRDY# are ACTIVE at the same time and AD[31:0] truly reflects the 4th-time SD[7:0], CPU can correctly complete current FETCH CODE CYCLE

When LATCHED mode is selected, four single-step executions (that is, the fifth single-step will be locked) have to be finished so the 7-segment display of PCI DATA BUS will show SD[7:0] of previous 4 steps

2.1> If TRANSPARENT mode is selected for main boards of this type, the 7-segment of TR-PCI DATA BUS may not correctly show DATA

The actual situation is illustrated as below:

ISA BUS		PCI BUS	
LA[23:20],SA[19:0]	SD[7:0]	PCI ADDRESS	PCI DATA
FFFFF0	EA	FFFFFFF0	????????
FFFFF1	5B	FFFFFFF0	????????
FFFFF2	E0	FFFFFFF0	????????
FFFFF3	00	FFFFFFF0	????????
FFFFF4	F0	FFFFFFF4	????????

2.2> If LATCHED mode is selected for main boards of this type, the 7-segment of TR-PCI DATA BUS can show correct DATA

Real situation is illustrated as below:

ISA BUS		PCI BUS	
LA[23:20],SA[19:0]	SD[7:0]	PCI ADDRESS	PCI DATA
FFFFF0	EA	FFFFFFF0	????????
FFFFF1	5B	FFFFFFF0	????????
FFFFF2	E0	FFFFFFF0	????????
FFFFF3	00	FFFFFFF0	????????
FFFFF4	F0	FFFFFFF4	00E05BEA

4>STEP-LPC

4-1> Product Features

It has a toggle switch that can be used to select Bear Technology Debug BIOS or User BIOS; it also has two LEDs to indicate which BIOS is selected.

It has a toggle switch that can be used to select Free RUN or Single-Step Executaion; it also has two LEDs to indicate which is selected.

It has a push button that can be used to conduct single-step tracing of the results of the execution of STEP-LPC Debug BIOS

When LPC type main boards(for example:intel 810,820 & SIS 630 & SIS 540) are to read ON Board 之 BIOS, STEP-LPC will issue DEVSEL# signals to PCI BMS, making chip set turn to read from STEP-LPC 之 BIOS. It can also set Single-Step Execution Funciton to trace Debug BIOS.

Bear Technology-degisned TRACE-PCI should be used to monistor the status of PIC BUS

4-2> Switch Settings

1> JP1: It isused to adjust PIC ADDRESS LATCH Timing.

1○○3 2-4(lower): PIC ALE DELAY(default setting)
2○○4

1○○3 1-3(upper): PCI ALE NORMAL
2○○4

2> SP1: It is used to select Debug BIOS.

switched up:(BEAR LED is lit)
select U18's Bear Debug BIOS

switched down:(USER LED is lit)
select U19's customized debug BIOS

3> SP2: It is used to select Free RUN /Single STEP function

switched up:(Free LED is lit)
select FREE PRN funciton

switched down:(STEP LED is lit)
select single-step execution function
* It should be used with PU1 button to trace step-by-step the status of PIC BUS

4>PU1: Single-Step Button
* It should be used the setting of SP2 Single Step Enable to trace step-by-step the status of PIC BUS

Chapter 2 How it Works and When to Use Debug Card

1> What is Single-Step Execution and a Interrupt Point?

What is Single-Step Execution?

1a> IBM-compatible main boards that have the specification are such that when ISA Cycle is genreted, IOCHRDY# will be made LOW and the ISA Cycle will be in WAIT STATE until IOCHRDY# is resumed to high voltage

1b> The Debug card is designed on the above-mentioned characteristic to execute the Single-Step and Interrupt functions

1c> This card can use STEP STEP TRIGGER button or RC drive to observe if the single-step execution of the main board is normal

What is Address Break?

2a> With the settings of SA[19:0], the Debug Card will compare SA[19:0] and the switch settings of ADDRESS BREAK, which both are sent from ISA SLOT.
If Address is identical and the COMMANDs sent from STEP COMMAND and ISA SLOT are the same, IOCHRDY# will become LOW and ready to enter WAIT STATE

2b> WAIT STATE can be cleared by STEP TRIGGER button or RC TRIGGER

What is Address+ DATA Break?

3a> When SA[19:0], SD[7:0] and COMMAND of ISA SLOT are identical to the setting of the Debug Card, the main board will enter WAIT STATE.

The differences between STEP TRIGGER 和 RC TRIGGER

4a> The following two ways can be used to clear the main board from WAIT STATE that come up in the wake of Single-Step or Break.

4b> STEP TRIGGER: manually push PU1 to clear current WAIT STATE

4c> RC TRIGGER: When RC TRIGGER is enabled, WAIT STATE will be automatically cleared 1/4 sec after the main board enters WAIT STATE.

Using Single-Step Function

5a> Single-Step is the most commonly-used and the simplest function

5b> Set STEP COMMAND to MEMR# and enable Single-Step, then on a normal main board you can see the following messages

ADDRESS	DATA
LA[23:20] SA[19:0]	SD[7:0]
FFFFF0	EA
FFFFF1	5B
FFFFF2	E0
FFFFF3	00
FFFFF4	F0
———	——

0FE058

5c> Using the messages of ADDRESS and DATA, preliminary judgement can be made on problems encountered.

Using Interrupt Point

6a> Interrupt Points are used widely; it requires higher skill to use and is favored by advanced users.

6b> Let's see the following examples:

Situation 1: Main board is found down at a certain ERROR CODE

Objective: To learn what ERROR CODEs have been gone through from the main board is started to the time it went down

Application 1: Set ADDRESS BREAKto 80H

Set STEP COMMAND to IOW#

Together with STEP or RC TRIGGER, the objective can be achieved

Situation 2: From ERROR CODE message to see that the error message is CMOS ERROR

Objective 2: To observe the Reading/Writing of CMOS PORT

Preparation 23: It needs to be understood that CMOS PORT is 70H and 71H

Application 2: Set ADDRESS BREAK to 70H and 71H

Set COMMAND to IOR# & IOW#

Together with STEP or RC TRIGGER, the objective can be achieved

Situation 3: VGA CARD fails

Objective 3: To observe if the first 32 Bytes of VGA BIOS are correct

Preparation 3: It needs to be understood that VGA BIOS address is 70H and 71H

Application 3: Set ADDRESS BREAK to C0000-C001F and COMMANDto MEMR#

Together with STEP or RC TRIGGER, the objective can be achieved

Objective 4: To understand a certain how BIOS is conducting a certain INDEX PROGRAN to the CHIP SET

Assumption 4:INDEX PORT : 22H INDEX : 50H

DATA PORT : 23H

Application 4:

1. Set ADDR BREAK to 22H and 23H
2. Set DATA BREAK to 50H
3. Set STEP COMMAND to IOW#
4. Boot
5. Stop at IOW# , I/O PORT 22H , DATA : 50H
6. DISABLE DATA BREAK switch
7. Press PU1 once
8. Stop at IOW# , I/O PORT 23H
9. From DATA BIOS 之 7 SEGMENT, the data written into PORT 23H can be observed

2> Principles of Debug Card

1>ISA Debug Card

> Origional IBM AT design is that normal 8 BITS I/O or MEMORY Cycle needs six ATCLK C, for example of 8MHZ, it needs about 750 msec.

>ISA SLOT provides a signal, IOCHRDY# so that if the device connected to ISA SLOT is slower and the access time for that device is longer (e.g., longer than 750 msec), then the current ISA Cycle can be extended with Active Low IOCHRDY#

> ISA single-step execution uses IOCHRDY#, which makes ISA generate WAIT STATE until IOCHRDY# resume to high voltage, ending current ISA cycle

> ISA single-step execution uses IOCHRDY#, which makes ISA generate WAIT STATE until IOCHRDY# resume to high voltage, ending current ISA cycle

2>TRACE-PCI Debug Card

> For main boards that don't support ISA SLOT, it becomes an issue how to trace the main board status during boot process with PCI SLOT

> When main board is reading BIOS DATA, PIC MEMORY READ cycle will be generated. And during the execution of current PCI cycle, Chip Set will send back PCI TRDY# (Active Low) and, during TRDY# Active period, put BIOS DATA to AD[31:0]

> Since Chip Set sees system BIOS as an ON-Board Device, when chipset decodes the message that CPU is to read BIOS DATA, it will take over the control and produce the Timing for BIOS to read. So it is very unlikely to intercept TRDY# sent back from Chip Set and BIOS DATA LOSS is likely to be caused if interception is attempted.

> For the above-mentioned reasons, TRACE-PCI will not try to intercept TRDY# but uses monitoring method and LATCH the ADDRESS & DATA of the N-th PCI cycle to the ADDRESS & DATA 7-Segment LED of TRACE-PCI.

> If the user has set TRDY# coumter=1 then, upon Hardware-RESET or booting, TRACE-PCI will display the ADDRESS & DATA of the first PCI cycle > In the same sense, TRDY# coumter=9 then, while resetting the main board, TRACE-PCI will display the ADDRESS & DATA of the 9th PCI cycle

(the followings are example made with GIGABYTE BXC main board)

TRDY# counter	PCI ADDRESS	PCI DATA
01	FFFFFFF0	00 E0 5B EA
02	FFFFFFF4	52 4D 2A F0
03	FFFFFFF8	00 02 2A 42
04	FFFFFFFC	FF FF 00 00
05	FFFFFFE0	00 00 00 00
06	FFFFFFE4	00 00 00 00
07	FFFFFFE8	39 36 41 32
08	FFFFFFEC	44 30 47 4B
09	000FE058	90 00 5A 55
0A	000FE05C	FC FA EA 8E
0B	000FE050	
0C	000FE054	

> The fore-mentioned TRDY# counter shows the number of TRDY# and TRDY# counter setting are the same after main board was RESET, and in this case, TRACE-PCI will LATCH the PCI ADDRESS & DATA of that time. So when you set a new value for TRDY# 之 counter, you need to reboot the machine or RESET the main board so as to catch the N-th PCI and have it displayed on the TRACE-PCI.

2>STEP-LPC Debug Card

> Generally there are two types of PCI main boards on the market

1> System BIOS is read through ISA BUS

For example: inter BX, SIS 55XX ,VIA , ALI main boards

2> System BIOS is read through LPC INTERFACE

For example: inter 810,820 & SIS 630 & SIS 540

* For the above-mentioned two types the main board BIOS is not read through ISA BUS

> The above two types both use PCI BUS to access BIOS. However, the second type does not access BIOS through ISA so ISA cannot be used to monitor BIOS ADDRESS & DATA

> Moreover, for the second type main board, during BIOS access cycle, PCI BUS has priority over LPC and the Active PCI DEVSEL# can take the control of BUS. But it is not the case with the first type main board.

> For second type main boardsBear Techonolgy has developed STEP-PCI debug card that incorporates TRACE-PCI, providing debuggin solution to popular intel 810,820 & SIS 630,540 series main boards

> Since STEP-LPC has priority over LPC BIOS, so when STEP-LPC is installed, the main board will read STEP-LPC BIOS and is unable to read LPC BIOS

> Since STEP-LPC has taken control over main board's BIOS cycle, while STEP-LPC is in single-step execution mode, STEP-LPC can decides the timing of TRDY# Active so that STEP-LPC's single-step drive button can now be used to check if the reading of STEP-LPC BIOS is correct. In this case, the main board needs not to be RESET again as it does when TRDY# Counter settings are changed for TRACE-PCI

3> Timing of Using Bear Techonology Debug Card

3-2> Using TRACE-PCI alone

A> When to Use: It can be used with main boards on which the system BIOS is controlled by ISA BUS

*It can be used on all main boards except intel 810,820,SIS 630 & 540 main boards

B> Usage

> Set ISA (MEMR# Single-Step Function) and observe step by step the status of system BIOS

> Set ISA (IOW# single-step function) and replace system BIOS with Bear Technology BIOS TR-ISA1.1M and check step by step the ADDRESS & DATA of ISA and determine possible cause of the problem.

3-2> Using TRACE-PCI alone

A> Timing of Use

1> When dealing with main boards that don't have a ISA slot

2> If main board has ISA slot but ISA single-step card can't perform single-step function, TRACE-PCI 之 TRDY#count function can be used to observe step by step the status of PCI BUS

B> Usage

> Set TRACE-PCI to TRDY# count function and observe step by step the status of system BIOS so as to understand the status of system BIOS reading.

> SetIOW# single-step function and replace system BIOS with Bear Technology BIOS TR-ISA1.1M and check step by step the ADDRESS & DATA of PCI BUS and determine possible cause of the problem.

3-3> Using TRACE-PCI with TR-ISA

A> When to Use: This method can be used with main boards that has ISA & PCI SLOT and on which the system BIOS is controlled by ISA BUS

B> Usage

> Set ISA (MEMR# single-step function) and set TRACE-PC (Free RUN function). Then use ISA single-step function to check step by step the status of ISA&PCI ADDRESS & DATA BMS to understand the status of the reading of system BIOS

> Set ISA (IOW# single-step function) and set TRACE-PC (Free RUN function) and replace system BIOS with Bear Technology BIOS. Then use ISA IOW# single-step function to check step by step the ADDRESS & DATA of ISA & PCI and determine possible cause of the problem.

3-3> Using TRACE-PCI with STEP-LPC

A> Timing of Use

1> This method is suitable for main boards that have a PCI slot and on which the system BIOS is controlled by LPC interface (for example: intel 810, 820 & SIS 630 ,540 main boards)

2> For above-mentioned types of main boards, when Bear Technology BIOS is to be used, system BIOS may needs to be removed since there is no IC base on the main board. In such case, STEP-LPC BIOS may be used to perform debugging BIOS.

B> Explanation: How to Use TRACE-PCE (the function of TRDY#counter)

How is the single-step function of STEP-LPC is different?

> The BIOS DATA caught while using TRACE-PCI (TRDY# counter function) is ON Board LPC BIOS. But the BIOS DATA caught while using STEP-LPC BIOS DATA of STEP-LPC.

> Therefore, even if STEP-LPC reads BIOS DATA, it does not mean LPC BIOS is correct.

> When it is unable to correctly read LPC BIOS using TRACE-PCE (TRDY# counter function), it is maybe PCI BMS or LPC interface that causes the problem

In this case, we can use single-step function of STEP-LPC to read STEP-LPC BIOS and check the status of PCI BUS

If PCI BUS is normal, then it is LPC interface that causes the problem or the On Board LPC BIOS has poor burn-in quality.

However, if PCI BUS is not functioning normal in the first place, then PCI BUS needs to be trobleshot as LPC interface will not be function correctly if PCI BUS has a problem.

C> Usage

> Set STEP-LPC to Single-Step

Set TRACE-PCI to Free RUN and DATA to PASS mode

Observe step by step the status of STEP-LPC BIOS

> Set STEP-LPC to Free RUN function

Set TRACE-PCI to IOW# single-step function

Control the push button of TRACE-PCI and check step by step the changes of PCI ADDRESS & DATA and judge the question points

Chapter 3 Pratical Examples

Example 1 > TR-ISA MEMR# Single-Step

Operation procedure and check points

. SP1: (ON) switched down SW4-2: (ON) switched right

. Boot

. Press PU1 …. (Check ISA ADDRESS & DATA & Status)

ADDRESS	DATA
LA[23:20] SA[19:0]	SD[7:0]
FFFFF0	EA
FFFFF1	5B
FFFFF2	E0
FFFFF3	00
FFFFF4	F0
———	——
0FE058	

Example 1-1

Example 2 > TR-ISA MEMR# Single-Step + RC TRIGGER

Operation procedure and check points

. SP1: (ON) switched down SP3 : (ON) switched down SW4-2: (ON) switched to right

. Boot

. Check ISA ADDRESS & DATA & Status every 1/4 sec.
The Changes are shown as below:

ADDRESS	DATA
LA[23:20] SA[19:0]	SD[7:0]
FFFFF0	EA
FFFFF1	5B
FFFFF2	E0
FFFFF3	00
FFFFF4	F0
———	——
0FE058	

Example 2-1

Example 3 > TR-ISA IOW# Single-Step

Operation procedure and check points

. : Switch down SP1(ON) Switch SW4-3 to the right (ON)

. Boot

. Press PU1 …. (check if ISA ADDRESS & DATA & IOW# LEDs are lit)

Example 3-1

Example 4 > TR-ISA IOR# Single-Step

Operation procedure and check points

Switch down SP1(ON) and Switch SW4-3 to the right (ON)

Boot

. Press PU1 …. (check if ISA ADDRESS & DATA & IOW# LEDs are lit)

Example 4-1

Example 5 > TR-ISA IOW# , 80H interrupt point

Operation procedure and check points:

. SP2: Switch down SP1(ON) and Switch SW4-3 to the right (ON). Set ADDRESS Break POINT = 80h Boot

. Press PU1 …. (check if ISA ADDRESS & DATA & IOW# LEDs are lit)

. Check if ISA ADDRESS is 80H and if IOW# LED is lit)

. Check if ISA DATA change in the order of BIOS POST CODE

Example 6 > TR-ISA IOW#/IOR# , 70H / 71H interrupt point

Operation procedure and check points:

. SP2: Switch down SP1(ON) and Switch SW4-3 to the right (ON). Set ADDRESS Break POINT = 80h

. Switch down(ON) SW2-1 (SA0 will not be compared)

. Boot

. Check if ISA ADDRESS is 70H or 71H and if IOW# or IOW# LED is lit)

. Press PU1

. Check if ISA ADDRESS is 70H or 71H and if IOW# or IOW# LED is lit)

Example 7 > TR-ISA IOW# , 80H ADDRESS interrupt point & DATA interrupt point (0DH)

Operation procedure and check points:

Switch down SP2&4(ON) and Switch SW4-3 to the right (ON)

. Set ADDRESS Break POINT = 80h and DATA Break Point = 0Dh

. Boot

. Check if ISA ADDRESS is 80H and if IOW# LED is lit)

. Check if ISA DATA is 0DH

Example 7-1

Example 8 > TRACE-PCI FREE RUN

Conditions: DRAM Module is not installed & Award BIOS ?

. Check if ERROR CODE is C1DH

Example 8-1

Example 9 > TR-ISA MEMR# Single-Step + TRACE-PCI FREE RUN

Function Used: TRACE-PCI Free Run + DATA (Latched Mode)

Conditions: ISA Single-Step

Operation procedure and check points:

. The settings of TR-ISA & TRACE-PCI are illustrated as below

. Boot

. Press (TR-ISA) PU1 and check ISA & PCI (ADDRESS & DATA & Status)

ISA BUS		PCI BUS	
LA[23:20],SA[19:0]	SD[7:0]	PCI ADDRESS	PCI DATA
FFFFF0	EA	FFFFFFF0	????????
FFFFF1	5B	FFFFFFF0	????????
FFFFF2	E0	FFFFFFF0	????????
FFFFF3	00	FFFFFFF0	????????
FFFFF4	F0	FFFFFFF4	????????

Example 9-1

Example 10> TRACE-PCI TRDY Count (Single-Step Tracing)

Function Used : TRACE-PCI TRDY COUNT + DATA (Latched Mode)

Condition : PCI TRDY Count (Single-Step Tracing)

Mian Board to be Debugged: MicroStar MS6182(intel 810 mainboard)

Operation procedure and check points:

. TRACE-PCI settings are illustrated as below

. Set TRDY COUNTER = 1

Boot or Hardware RESET and check PCI (ADDRESS & DATA & Status)

PCI ADDRESS	PCI DATA
FFFFFFE0	00000000

. Set TRDY COUNTER = 2

Boot OR Hardware RESET and check PCI (ADDRESS & DATA & Status)

PCI ADDRESS	PCI DATA
FFFFFFE4	00000000

TRDY COUNTER	PCI ADDRESS	PCI DATA
1	FFFFFFE0	00000000
2	FFFFFFE4	00000000
3	FFFFFFE8	39364136
4	FFFFFFEC	39344D4D
5	FFFFFFF0	00E05BEA
6	FFFFFFF4	524D2AF0
7	FFFFFFF8	00022A42
8	FFFFFFFC	FF600000
9	000FE040	0D2E636E
A	000FE044	42422A0A
B	000FE048	002A5353
C	000FE04C	00000000
D	000FE050	00000000
E	000FE054	00000000
F	000FE058	90005B55

Example 10-1

Example 11> STEP-LPC (Single-Step Tracing) + TRACE-PCI (FREE RUN)

Functions Used : STEP-LPC (single-step) + [TRACE-PCI (FREE RUN) + DATA (PASS Mode)]

Condition : STEP-LPC (single-step tracing)

Mian Board to be Debugged: MicroStar MS6182(intel 810 mainboard)

Operation procedure and check points:

. Settings for STEP-LPC & TRACE-PCI are illustrated as below …

Boot or Hardware RESET and check PCI (ADDRESS & DATA & Status)

Press PU1 of STEP-LPC and conduct single-step tracing of PCI (ADDRESS & DATA & Status)

Action	PCI ADDRESS	PCI DATA
PWR_ON or H_RESET	FFFFFFE0	FFFFFFFF
Press PU1 once	FFFFFFE4	FFFFFFFF
Press PU1 once	FFFFFFE8	FFFFFFFF
Press PU1 once	FFFFFFEC	FFFFFFFF
Press PU1 once	FFFFFFF0	000000EA
Press PU1 once	FFFFFFF4	776655F0
Press PU1 once	FFFFFFF8	BBAA9988
Press PU1 once	FFFFFFFC	FFEEDDCC
Press PU1 once	000F0000	B00300BA
Press PU1 once	000F0004	9090EE00

The above is the Bear Technology Debug BIOS CODE

例 12> STEP-LPC (FREE RUN) + TRACE-PCI (IOW# Single-Step Tracing)

Functions Used: STEP-LPC (FREE RUN) (Execute Bear Tenology Debug BIOS { TR-ISA1.1M})
+ TRACE-PCI (IOW# Single-Step Tracing)+ DATA (PASS Mode)]

Conditions : STEP-LPC (FREE RUN) + TRACE-PCI (IOW# Single-Step Tracing)

Mian Board to be Debugged: MicroStar MS6182 (intel 810 mainboard)

Operation procedure and check points:

. Settings for STEP-LPC & TRACE-PCI are illustrated as below …

Boot or Hardware RESET and check PCI (ADDRESS & DATA & Status)

Press PU1 of TRACE-PCI and conduct single-step tracing of PCI (ADDRESS & DATA & Status)

Actions	PCI ADDRESS	PCI DATA
PWR_ON or H_RESET	00000300	??????00
Press PU1 once	00000301	????11??
Press PU1 once	00000302	??22????
Press PU1 once	00000303	33??????
Press PU1 once	00000304	??????44
Press PU1 once	00000305	????55??
Press PU1 once	00000306	??66????
Press PU1 once	00000307	77??????
Press PU1 once	00000300	????0000
Press PU1 once	00000302	0000????
Press PU1 once	00000304	????0000
Press PU1 once	00000306	0000????

The above is the Bear Technology Debug BIOS CODE